Design of electro-optical flip-flop

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Abstract

The neuromorphic photonic circuits have the potential to generate a wide variety of devices or systems with specialized functions. In our previous work, we proposed an electro-optical architecture to form the logic gates. Electro-optical AND, OR, NAND, NOR, XOR and XNOR logic gates could be realized in the structure by tuning the parameters of the electro-optical devices. In this work, we design the electro-optical flip-flop with two electro-optical logic gates. The electro-optical logic gates are built by means of Multilayer Perceptron using directional couplers, phase modulators and optical amplifiers. The truth value of the input signal 0 or 1 is determined by the applied voltage, 0V or 1V, on the two phase modulators, respectively. We also assess the tolerance of the system by calculating the visibility of the output signals with 1% error due to the fabrication error of the optical components. The simulation results show that the minimum visibility of the logic gates and the flip-flop are 0.91 and 0.98, respectively indicating that the electro-optical flip-flop can be realized even with the fabrication errors.

Keywords: optical memory, optical logic gates, optical flip-flop, optical latch, multilayer perceptron.

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Introduction

Optical memory is a significant portion for optical computing. Many efforts have been devoted to realize the all-optical memory [1]. Over the few decades, optical memory with photonic crystals [2, 3], micro-resonators [4], holography [5-7] or phase change materials [8] were demonstrated. The light source used in optical memory could be femtosecond laser to induce the birefringence [9], or the serially interconnected lasers to compensate the coupling losses [10]. To increase the time that data been preserved, a loop structure is commonly employed [11] in which the output signal is reinserted into the optical memory. Some studies about all-optical flip-flop (AOFF) using loop structure have been done [12, 13]. Other research groups also proposed the AOFF utilizing bistability to yield a set-reset flip-flop operation which is controlled by the external light sources at different wavelengths [14]. AOFFs with high on-off contrast ratio [15], high-speed operation [16] and ability for integration [17] have been realized. With these advantages, AOFF can serve as the fundamental building blocks to achieve more advanced functionalities, such as optical packet switching or optical clock generation [15, 16].

Recently, the artificial intelligence algorithm has been widely using the neural networks with nonlinear system [18]. Some groups have demonstrated a nonlinearity equalizer based on the multilayer perceptron (MLP) which is a modern feedforward neural network consisting of fully connected neurons with nonlinear activation functions [19]. In our previous work, we have reported experimentally the neural networks in a silicon photonics chip. The input triangular and rectangular input optical wave packets can be distinguished [20]. Based on the optical neural networks [21, 22], we also proposed the reconfigurable optical logic gates [23]. The structure is designed by the MLP to establish the electro-optical (EO) logic gates which consist of optical amplifiers, directional couplers (DCs), and phase modulators (PMs). The light source was a continuous-wave laser source at the wavelength of 1550 nm. The logic 0 or 1 is determined by applying the voltages on the phase modulators to shift the phase of the light signals. The OR, XOR, AND, NAND, NOR, and XNOR logic gates can be achieved with a single optical architecture [24]. In the present work, we use two NAND logic gates developed in Ref. [23] to build the EO flip-flop which is the basic structure of memories in electronics. The signal passing through the one logic gate is injected into the input port of another logic gate. The state of the signal can be kept in the electro-optical memory as long as the laser source is provided. The electro-optical memories could be used in the optical computing system for data storage.

1. Electro-optical logic gates and flip-flop

Fig. 1 depicts the structure of the NAND logic gate. The CW laser source at the wavelength of 1550 nm with the power of 0.1W is injected into the DC_{in} to split the light source into two light beams. The general formula of the output fields , X_{out1} and X_{out2}, of the 2-by-2 directional couplers with the coupling ratio of α as the two input electric fields are X_{in1} and X_{in2}, respectively can be expressed by

$$\begin{bmatrix} X_{out1} \\ X_{out2} \end{bmatrix} = \begin{bmatrix} \sqrt{1-\alpha} & i\sqrt{\alpha} \\ i\sqrt{\alpha} & \sqrt{1-\alpha} \end{bmatrix} \begin{bmatrix} X_{in1} \\ X_{in2} \end{bmatrix}. \quad (1)$$

The coupling ratio of DC_{in} is 50 %. The two light beams are launched into two PMs (as shown by PM_A and PM_B in Fig. 1). The output field of the phase modulators with the phase delay of ϕ can be given by.

$$X_{out}=X_{in}e^{i\phi}. \quad (2)$$

The half-wave voltage Vπ of PM_A and PM_B is set to be 1V and 2V, respectively. The voltages applied on the PMs are 0V or 1V representing the logic 0 and 1, respectively. The output signals of PM_A and PM_B are launched into DC_A. DC_A is connected to DC_B and DC_C. The signals are split into four light beams. The coupling ratio of DC_A, DC_B and DC_C are chosen randomly, respectively. The output signals of DC_B and DC_C are connected to four optical amplifiers A_1, A_2, A_3 and A_4, respectively. The gain of the optical amplifier is given by

$$G=\frac{G_0}{1+G_0\frac{P}{P_{SAT}}}, \quad (3)$$

where G_0, P_{SAT}, P are the small signal power gain, the saturation output power, the average power of input light, respectively. In our MLP architecture, the activation function is obtained by using the amplifiers in which the power of the input signal is amplified non-linearly. In our structure, G_0 and P_{SAT} are set to be 31.27 dB and 30 dBm, respectively. The output of the logic gate is obtained as the four output optical signals of the amplifiers pass through DC_1, DC_2, DC_3 and PM_1, PM_2, PM_3.

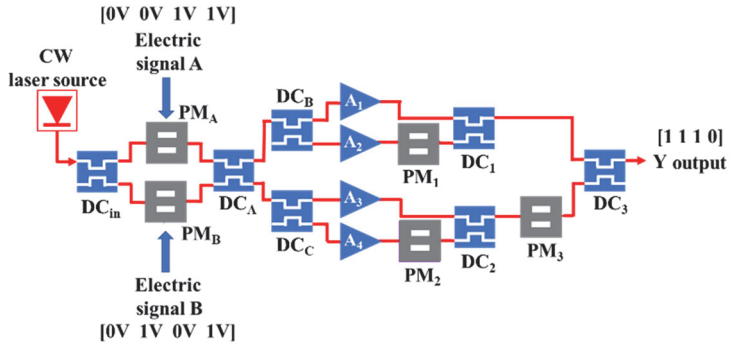

Fig. 1. The structure of the NAND gate that we used to build up the flip-flop. The voltage applied on the PMs is 0V or 1V representing logic 0 and 1, respectively. The four input combinations of voltages applied on PM_A and PM_B are (0V, 0V), (0V, 1V), (1V, 0V) and (1V, 1V), respectively. The corresponding outputs of the NAND logic gate are 1V, 1V, 1V and 0V, respectively

The target output of the NAND gate Y^{target} can be given by

$$Y^{target}=W^{out}X, \quad (4)$$

where $W^{out}=[w_1, w_2, w_3, w_4]$. The 1-by-4 matrix W^{out} represents the three directional couplers DC_1, DC_2 and DC_3 and the three phase modulators PM_1, PM_2 and PM_3. For NAND gate, the logic of the target output Y^{target} is a 1-by-4 matrix [1, 1, 1, 0] as the input logic is [(0, 0), (0, 1), (1, 0), (1, 1)], respectively. The X in Eq. (4) is a 4-by-4 matrix. The 16 element values of the X are obtained by collecting the complex electric fields of the output light of the four amplifiers A_1, A_2, A_3 and A_4 as the input logic is [(0, 0), (0, 1), (1,0), (1,1)], respectively. We can obtain W^{out} by using the inverse of the matrix X which can expressed by

$$W^{out}=Y^{target}X^{-1}. \quad (5)$$

With Eqs. (1), (2), (4) and (5), we can derive the complex electric field of the output light of the logic gate as

$$Y=\sqrt{1-\alpha_3}\sqrt{1-\alpha_1}X_1+i\sqrt{1-\alpha_3}\sqrt{\alpha_1}\,e^{i(\phi_1)}X_2+i\sqrt{\alpha_3}\sqrt{1-\alpha_2}\,e^{i(\phi_3)}X_3-\sqrt{\alpha_3}\sqrt{\alpha_2}\,e^{i(\phi_2+\phi_3)}X_4, \quad (6)$$

where α_1, α_2, α_3 and ϕ_1, ϕ_2, ϕ_3, are the coupling ratio of DC_1, DC_2, DC_3 and the phase delay of PM_1, PM_2, PM_3, respectively. X_1, X_2, X_3 and X_4 are the output of the activation function provided by the amplifiers. The output light Y is the linear combination of the X_1, X_2, X_3 and X_4 to form the MLP architecture. The coefficients of the terms X_1, X_2, X_3 and X_4 corresponds to the four values of w_1, w_2, w_3 and w_4 of W^{out} forming four simultaneous equations to obtain α_1, α_2, α_3 and ϕ_1, ϕ_2, ϕ_3 by limiting $0<\alpha_1, \alpha_2, \alpha_3<1$ and $-180^o\leqq\phi_1, \phi_2, \phi_3\leqq 180^o$. For the NAND gates, the coupling ratio of DC_A, DC_B and DC_C are chosen randomly to be 0.41, 0.82 and 0.11, respectively. α_1, α_2, α_3 and ϕ_1, ϕ_2, ϕ_3 are obtained to be 0.59, 0.51, 0.73 and 3.43°, 7.61°, – 3.01°, respectively.

Fig. 2 illustrates the structure of the EO flip-flop in which the two NAND gates presented in Fig. 1 are replaced by the blocks to simplify the figure. The parameters of the phase modulators and the directional couplers of the two NAND gates are identical in the EO flip-flop. One electric input port of each NAND gate serves as the input port of the system which is the set and the reset of the EO flip-flop, respectively. The other electric input ports are connected to the output port of the flip-flop, forming a loop structure. The output signal of the two NAND gates are connect to the photo detectors to convert the optical output signals to electrical signals. After amplifying the electric signals, the output of the EO flip-flop, the signals Q and $\bar{Q}$, are obtained. The electrical output signals are also applied on the NAND gates to form the loop.

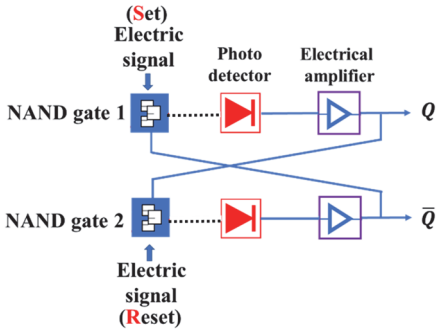

Fig. 2. The structure of the EO flip-flop. NAND gates are replaced by one block. The dotted and solid lines represent the optical fibers and the electric cables, respectively

2. Method

The devices parameters for the NAND gate reported in Ref. [23] are applied in this study. The coupling ratio of the diectional couplers in Fig. 1 for DC_A, DC_B, DC_C, DC_1, DC_2 and DC_3 is 22 %, 8 %, 7 %, 47 %, 55 % and 74 %, respectively. The phase delay for the phase modulators PM_1, PM_2 and PM_3 in Fig. 1 is 0.46°, 5.82°, and – 8.27°, respectively.

In Fig. 2, the output signals of the photodetectors are amplified to obtain Q and $\bar{Q}$ and applied on the NAND gates. The amplification of the amplifiers is set to be 37.71 dB.

The rise time and fall time for the phase modulators, the response time of the amplifiers and the photodetectors may induce the delay to change the state for the output Q and $\bar{Q}$ of the EO flip-flop. For the phase modulators, the rise time and fall time of 10 ps have be reported [25]. The gain recovery time of the optical amplifiers and the response time of electronic amplifiers can be as short as 5 ps [26] and 10 ps [27], respectively. The photodetectors with the response time of 1.3 ps have been demonstrated [28]. In our EO flip-flop with the loop structure, the light should pass through the two NAND gates (NAND gates 1 and 2 in Fig. 2) to complete the state change for Q and $\bar{Q}$. For one NAND gate, the signal should pass three phase modulators, one optical amplifier, one electronic amplifier and one photodetector. The delay time of one NAND gate is estimated by summing the response times for all devices to be about 46.3 ps. To change the states of the electric output Q and $\bar{Q}$, the signals should pass two NAND gates due to the loop structure, the delay time is about $T_d = 92.6$ ps.

3. Simulation Results

We calculate the output voltages of Q and $\bar{Q}$ as the light passing through the EO flip-flop. The time step is set to be 46.3 ps. We change the state of S and R for every $2T_d$. Fig. 3 shows the output voltages of Q and $\bar{Q}$. For a NAND gate, if any input is low, a high output results. We assume that 0V is applied on all electric inputs for both NAND gates for the initial state (Time = 0 ns). After the two light beams of the light sources pass respectively through the NAND gates 1 and 2, Q and $\bar{Q}$ are 1V as shown schematically in Fig. 3*a* and *b*.

In Fig. 3*a*, for every $2T_d$, the input signals are changed sequentially from [S, R] = [0V, 1V], [S, R] = [1V, 1V], [S, R] = [1V, 0V] to [S, R] = [1V, 1V] and then repeated. For the first $2T_d$, since S = 0V which is applied on the NAND gate 1, the output of Q is 1V. The input signal 1 is "written" into the EO flip-flop. Since R = 1V and Q = 1V which are applied on the NAND gates 2, the state of $\bar{Q}$ is changed to be 0V.

For the second $2T_d$, the input signal S is changed to = 1V. R is kept to be 1V. The state of Q is 1V since the electric inputs of the NAND gate 1 are S = 1V and $\bar{Q}$ = 0V. $\bar{Q}$ is kept to be 0V, since both the electric inputs of the NAND gate 2 are 1V. The states of the EO flip-flop are identical to the previous ones. The states of the first $2T_d$ are kept or so-called "memorized" during the second $2T_d$.

For the third $2T_d$, the input signal S keeps to be 1V. R is changed to be 0V which is applied on the NAND gate 2. $\bar{Q}$ is changed to be 1V. Q is changed to 0V since both the electric inputs of the NAND gate 1 are 1V. The signal switch happens first on $\bar{Q}$ for a delay time of 46.3 ns. Q is then changed for a delay time of 46.3ns. The total T_d is 92.6 ns which is schematically illustrated in Fig. 3*a*.

For the fourth $2T_d$, S is kept to be 1V. $\bar{Q}$ is unchanged to be 1V. R is changed to be 1V. Q is unchanged to be 0V. The states of the EO flip-flop are identical to those for the third $2T_d$. The states of the third $2T_d$ are memorized during the fourth $2T_d$.

For the fifth $2T_d$, since S is changed to be 0V, Q is changed to 1V. Since R is kept to be 1V with Q = 1V, $\bar{Q}$ is changed to be 0V.

In Fig. 3*b*, for the initial state (Time = 0 ns), we also assume that 0V is applied on all electric inputs for both NAND gates. Q and $\bar{Q}$ are 1V. For every $2T_d$, the input signals are changed sequentially from [S, R] = [1V, 0V], [S, R] = [1V, 1V], [S, R] = [0V, 1V] to [S, R] = [1V, 1V] and then repeated. For the first $2T_d$, R is kept to be 0V, $\bar{Q}$ is kept to be 1V. S is set to be 1V. Q is changed to be 0V. For the second $2T_d$, S = R = 1V the states of Q and $\bar{Q}$ are memorized in the EO flip-flop. For the following switch conditions, the same results are schematically illustrated in Fig. 3*a*.

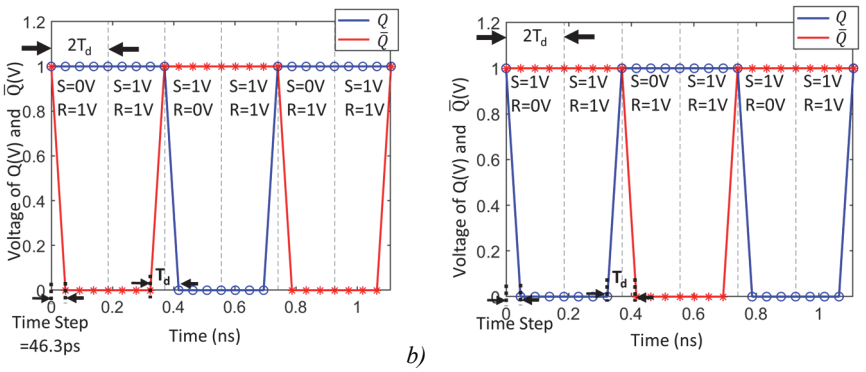

Fig. 3. Q and $\bar{Q}$ by varying S and R sequentially (a) from S, R = 0V,1V, S, R = 1V,1V, S, R = 1V,0V to S, R = 1V,1V and then the signals S and R are repeated. (b) from S, R = 1V, 0V, S,R = 1V,1V, S,R = 0V,1V to S,R = 1V,1V and then the signals S and R are repeated

Tab. 1 lists the value of the output signals of the EO flip-flop Q and $\bar{Q}$ with different combinations of input voltages S and R. The 0V for both S and R are not allowed, because both the output of Q and $\bar{Q}$ will be 1V which is not complementary. When S and R are applied by 0 and 1V, respectively, the corresponding output signals Q and $\bar{Q}$ will be 1 and 0V, respectively. When S and R are changed to 1 and 0V, respectively, the Q and $\bar{Q}$ will then become 0 and 1V. If S and R are both applied by 1V, the state of the EO flip-flop will be kept as previous state. Therefore, the EO flip-flop can be served as the EO memory.

Tab. 1 The values of the two outputs Q and $\bar{Q}$ of the EO flip-flop for different combinations of the input signals S and R

S	R	Q	$\bar{Q}$
0V	0V	Not allowed	
0V	1V	1V	0V
1V	0V	0V	1V
1V	1V	Q	$\bar{Q}$

To assess the tolerance of our system, the visibility of the output signals for the NAND logic gate (V_g) and flip-flop (V_f), respectively are expressed by

$$V_g = \frac{I^1_{min} - I^0_{max}}{I^1_{min} + I^0_{max}}, \tag{7}$$

$$V_f = \left|\frac{Q-\bar{Q}}{Q+\bar{Q}}\right|, \tag{8}$$

where the I^1_{min} is the minimum light intensity of the high level output signals, and the I^0_{max} is the maximum light intensity of the low level output signals of the NAND gate. Q and $\bar{Q}$ are the two output signals of the EO flip-flop.

Due to the manufacturing error of the directional couplers and the phase modulators, 1 % error of the coupling ratio and the phase delay may occur. We calculate the visibility of the logic gate and the EO flip-flop with 1 % error of the DCs and the PMs by increasing the coupling ratio and the phase delay by 1 %. For example, the coupling ratio of DC_1 is increased from 59 % to 60 %, and the phase delay of PM_1 is increased from 3.43° to 7.03° (3.6 = 1 % from –π to π). We choose the value of coupling ratio of DC_A, DC_B, and DC_C randomly for 10000 times and calculate the visibility with the 1% error of each DCs and PMs to find the lowest visibility. The results of the NAND gate and the flip-flop are listed in Tab. 2 and 3, respectively. For 1 % error of DCs and PMs in NAND gate, the worst visibility is 0.91. For the EO flip-flop, the worst visibility is 0.98. The results show that even with the manufacturing errors, the EO flip-flop with high visibility can be realized. In this study, the EO flip-flop can also be called $\overline{SR}$ NAND latch. The NAND gates could also be reconfigured to be NOR gates [23]. The SR NOR latch could also be realized in our system.

Tab. 2. The visibility of the output signals of the NAND gate V_g for 1% error of coupling ratio of directional couplers DC_{in}, DC_A, DC_B, DC_C, DC_1, DC_2, and DC_3 as well as the phase delay of the phase modulators PM_1,PM_2 and PM_3

	α_{in}	α_A	α_B	α_C	α_1	α_2	α_3	$\varnothing_1$	$\varnothing_2$	$\varnothing_3$
V_g	0.94	0.93	0.93	0.93	1	0.99	1	0.95	0.91	1

Tab. 3. The visibility of the output signals of the EO flip-flop V_f for 1% error of coupling ratio of directional couplers DC_{in}, DC_A, DC_B, DC_C, DC_1, DC_2, and DC_3 as well as the phase delay of the phase modulators PM_1,PM_2 and PM_3

	α_{in}	α_A	α_B	α_C	α_1	α_2	α_3	$\varnothing_1$	$\varnothing_2$	$\varnothing_3$
V_f	1	1	1	1	0.99	0.98	1	1	1	1

For the recent hot storage technology, the time for data writing into the SRAM is around 1ns [29]. The present structure could provide an ultra-short time for data writing of around 46.3 ps which is much shorter than that of modern SRAM.

4. Conclusions

In this work, an EO flip-flop (memory) with two EO NAND logic gates has been demonstrated. The values of coupling ratio and the phase delay of DC_1, DC_2, DC_3 and PM_1, PM_2, PM_3 are calculated by solving the simultaneous equations based on the multilayer perceptron. The states of the output signals can be kept as long as we supply the CW laser source and voltage source. We also calculate the visibility of the logic gate and flip-flop with 1 % error to assess the tolerance of the system. The results show that the flip-flop with high visibility can be achieved even with the fabrication errors.

With the MLP architecture, the input signals could be replaced by optical signals using phase modulation. The all-optical logic gates and memories could be achieved.

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